UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,156	01/20/2004	Stephen Paul Wilcox	104969-50921 (302715)	2563

26345 7590 05/04/2006

GIBBONS, DEL DEO, DOLAN, GRIFFINGER & VECCHIONE
1 RIVERFRONT PLAZA
NEWARK, NJ 07102-5497

EXAMINER	
LAM, NELSON C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,156	WILCOX ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication on 01/20/2004. Application 10/761,156 has been examined. In the examination of 10/761,156, claims 1-24 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-24 are rejected under 35 U.S.C. 102(e)** as being anticipated by Beletsky (US Patent No. 6,681,377).

As per **claim 1**, Beletsky discloses a method of determining a clock gating function for each of a set of clocked state-holding elements, wherein the elements have at least one common input and the method comprises the steps of:

a. determining, for each element, the conditions under which the element will hold its current value based only on the common inputs (Abstract; col. 3, line 20-27; col. 3, line 43-48; Fig. 1, #400; col. 6, line 21-32); and

b. combining, for each element, the determined conditions to form the clock gating function for that element (Abstract; col. 3, line 15-27; Fig. 1, #100, #200; col. 4, line 45-55; col. 5, line 5-20).

As per **claim 2**, Beletsky discloses the method according to claim 1, further comprising the step of, for each element, defining a Boolean function comprising variables forming the input to each element (Fig. 1, #400; col. 6, line 21-47).

As per **claim 3**, Beletsky discloses the method according to claim 2 wherein the step of determining the conditions under which the element will hold its current value is based on said Boolean functions (Fig. 1, #400; col. 6, line 21-47).

As per **claim 4**, Beletsky discloses the method according to claim 2 wherein the Boolean function is limited to the variables being common to the inputs of all elements (Fig. 1, #400; col. 6, line 21-47).

As per **claim 5**, Beletsky discloses the method according to any one of claim 2, further comprising the steps of:

determining a first set of variables that are common to logic functions forming the input to all elements (Fig. 1, #200; col. 5, line 21-33); and determining a second set of variables that are not common to logic functions forming the input to all elements, such that, in tracing back an input of any element, a variable of each set is always found (Fig. 1, #100; col. 4, line 62-67).

As per **claim 6**, Beletsky discloses the method according to claim 5 wherein the step of defining the Boolean function for each element is dependent upon those variables in the first and second sets (col. 5, line 21-33).

As per **claim 7**, Beletsky discloses the method according to claim 5 wherein the step of defining the Boolean function for each element is dependent only upon those variables in the first set (col. 5, line 21-33).

As per **claim 8**, Beletsky discloses a method according to claim 7, wherein the step of defining the Boolean function for each element further comprises the steps of defining a Boolean function in dependence on those variables in the first sets, and subsequently eliminating those variables in the second set (Fig. 1, #100; col. 4, line 62-67).

As per **claim 9**, Beletsky discloses the method according to any one of claim 5 wherein the step of determining the first and second sets of inputs comprises the steps of:

a. defining an input cone for each element, each input cone being determined by tracing back from the input of its respective element through a predetermined number of gates, and entering all variables located in that input cone (Fig. 1, #100; col. 4, line 62-67);

b. determining variables in the input cones that are common to all input cones (Fig. 3; col. 5, line 34-46);

c. tracing back from each element until any common variable is found, wherein all common variables found define a first set of variables (Fig. 1, #400; col. 6, line 21-47);

d. tracing back from each element until a variable in the first set is found, wherein all such traced back variables define a set L (Fig. 1, #400; col. 6, line 21-47);

e. defining a set M which comprises all variables in the input cones that are not included in set L (col. 6, line 51-56); and

f. tracing back from each element until a variable in the set M is found, wherein all variables that can be so traced back define a second set of variables (col. 6, line 57-67).

As per **claim 10**, Beletsky discloses the method according to claim 9 wherein a maximum size is allocated to the first set, further comprising the step of terminating the step c) if said maximum size is reached (col. 5, line 21-33).

As per **claim 11**, Beletsky discloses the method according to claim 9 wherein the tracing of an input path is terminated in step c) if a common variable is identified (col. 6, line 21-47).

As per **claim 12**, Beletsky discloses the method according to claim 9 wherein the tracing of an input path is terminated in step c) if a variable not in an input cone is identified (col. 5, line 52 to col. 6, line 4).

As per **claim 13**, Beletsky discloses the method according to claim 2 wherein the method is enabled responsive to the Boolean function for each element being dependent upon the output of that element (col. 8, line 32-43).

As per **claim 14**, Beletsky discloses the method according to claim 1 wherein the conditions are combined in an AND function (col. 6, line 33-47).

As per **claim 15**, Beletsky discloses the method according to claim 1 further comprising the step of creating a gate structure corresponding to the combined conditions (col. 4, line 45-55; col. 5, line 5-20).

As per **claim 16**, Beletsky discloses the method according to claim 2 further comprising the step of, for each element, determining a revised Boolean function which provides the same result as the defined Boolean function when the gating function has a logical value of 1 (col. 6, line 57 to col. 7, line 10).

As per **claim 17**, Beletsky discloses the method according to claim 16 further comprising the step of selectively replacing a defined Boolean function with a revised Boolean function in dependence upon a comparison of each defined and revised Boolean function to determine the most efficient function (col. 10, line 28-33).

As per **claim 18**, Beletsky discloses the method according to claim 17 wherein the most efficient function is the one that can be implemented with a smaller number of implementations in terms of logical gates (col. 10, line 28-33).

As per **claim 19**, Beletsky discloses a computer program product comprising a computer program code (col. 15, line 63-64; col. 16, line 22-39) for determining a clock gating function for each of a set of clocked state-holding elements, wherein the elements have at least one common input and the method comprises the steps of:

a. determining, for each element, the conditions under which the element will hold its current value based only on the common inputs (Abstract; col. 3, line 20-27; col. 3, line 43-48; Fig. 1, #400; col. 6, line 21-32); and

b. combining, for each element, the determined conditions to form the clock gating function for that element (Abstract; col. 3, line 15-27; Fig. 1, #100,#200; col. 4, line 45-55; col. 5, line 5-20).

As per **claim 20**, Beletsky discloses an apparatus (Fig. 12; col. 15, line 26-38) for determining a clock gating function for each of a set of clocked holding state elements, wherein the elements have at least one common input and the apparatus comprises:

a. means for determining, for each element, the conditions under which that element will hold its current value based only on the common inputs (Abstract; col. 3, line 20-27; col. 3, line 43-48; Fig. 1, #400; col. 6, line 21-32); and

b. means for combining, for each element, the determined conditions to form the gating function for that element (Abstract; col. 3, line 15-27; Fig. 1, #100,#200; col. 4, line 45-55; col. 5, line 5-20).

As per **claim 21**, Beletsky discloses the apparatus according to claim 20, further comprising means for defining, for each element, a Boolean function comprising the variables forming the input to each element (Fig. 1, #400; col. 6, line 21-47).

As per **claim 22**, Beletsky discloses the apparatus according to claim 20 further comprising: means for determining a first set of variables that are common to logic functions forming the input to all elements; and means for determining a second set of variables that are not common to logic functions forming the input to all elements, such that in tracing back an input of any element, a variable of each set is always found (Fig. 1, #100; col. 4, line 62-67).

As per **claim 23**, Beletsky discloses the apparatus according to claim 22 comprising:

a. means for defining an input cone for each element, each input cone being determined by tracing back from the input of its respective element through a predetermined number of gates, and entering all variables located in that input cone (Fig. 1, #100; col. 4, line 62-67);

b. means for determining variables in the input cones that are common to all input cones (Fig. 3; col. 5, line 34-46);

c. means for tracing back from each element until any common variable is found, wherein all common variables found define a first set of variables (Fig. 1, #400; col. 6, line 21-47);

d. means for tracing back from each element until a variable in the first set is found, wherein all such traced back variables define a set L (Fig. 1, #400; col. 6, line 21-47);

e. means for defining a set M which comprises all variables in the input cones which are not included in set L (col. 6, line 51-56); and

f. means for tracing back from each element until a variable in the set M is found, wherein all variable that can be so traced back define a second set of variables (col. 6, line 57-67).

As per **claim 24**, Beletsky discloses a computer system (Fig. 12, #1120; col. 15, line 26-33) comprising the apparatus for determining a clock gating function for each of

a set of clocked holding state elements, wherein the elements have at least one common input and the apparatus comprises:

a. means for determining, for each element, the conditions under which that element will hold its current value based only on the common inputs (Abstract; col. 3, line 20-27; col. 3, line 43-48; Fig. 1, #400; col. 6, line 21-32); and

b. means for combining, for each element, the determined conditions to form the gating function for that element (Abstract; col. 3, line 15-27; Fig. 1, #100, #200; col. 4, line 45-55; col. 5, line 5-20).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on Monday-Friday from 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nelson Lam

Nelson Lam
Assistant Examiner
Art Unit 2825

A. M. Thompson
Primary Examiner
Technology Center 2800